International Journal of Computer Science and Business Informatics

IJCSBI.ORG

A New Current-Mode Geometric-Mean Structure for SRD Filters

Ebrahim Farshidi and Saman Kaiedi
Electrical Department, Faculty of engineering,
Shahid Chaman University of technology,
Ahvaz, Iran

ABSTRACT

A current-mode square-root domain filter based on a new geometric-mean circuit is presented. The circuit is a tunable first-order low pass filter, working in low voltage, and featuring low nonlinearity. It employs MOSFETs that operate in both strong inverted saturation and triode regions. Simulation results by HSPICE confirm the validity of the proposed design technique and show high performance of the proposed circuit.

Keywords

Current-mode, Geometric-mean, squarer/divider, Companding, Filter.

1. INTRODUCTION

Companding process (compressing and expanding) as an attractive technique in analog circuit designs have drawn the attention of many researchers. In a filter employing companding technique, the circuit is internally nonlinear and the dynamic range (DR) of its signal is different at various points of signal path, and still, the resulting input-output current relationship is linear. The main advantage of these filters is their large dynamic ranges in low voltages, caused by voltage swing reduction at internal nodes. The first implementation of companding systems employed the exponential I-V characteristic of bipolar transistors that led to the log-domain structures [1, 2]. Developments in CMOS circuits and also similarity in I-V characteristics, caused the bipolar transistors were substituted by MOS transistors operating in weak inversion region [3]. However, the effects of limited speed and transistor mismatches restricted their applications. Afterwards, companding systems employed MOS transistors in saturation region based on voltage translinear principle and class-AB linear transconductors that led to Square-Root-Domain (SRD) structures [4-14]. The main drawback of these topologies is that for correct operation, all MOS transistors of the circuit must work in saturation region. If, in some conditions, the transistors are forced to enter in triode region, it will invalidate the MOS translinear or transconductance principle. This

restricts the input range and affects the linearity. In this work to overcome the above problems in SRD filter, a new approach in which MOS transistors operate both in saturation and triode regions is proposed [15]. The simulation results of the proposed circuit show less nonlinearity and less total harmonic distortion (THD) compared to those reported before [4]-[8].

This paper is organized as follows. In section 2, the basic principle of current-mode SRD filter operation is presented. In section 3 a divider-square root-multiplier (DSM), as the basic building block of the filter, is presented. This DSM has been realized by using of a new geometric-mean circuit. In section 4 a current-mode first-order LPF is designed. The simulation results of the filter show that the circuit has favorable characteristics.

2. BACKGROUND STUDY

In a current-mode first-order low pass filter and in Laplace domain, the output current I_{out} and input current I_{in} are related as:

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{A}{1+\frac{s}{\omega_c}} \tag{1}$$

in which, A is the DC gain and $\omega_c = \frac{1}{\tau}$ is the cutoff frequency of the filter. In time domain eqn. (1) can be written as:

$$\tau \frac{dI_{out}}{dt} + I_{out} = AI_{in}\,. \tag{2}$$

Also in the circuit shown in Figure 1, the I-V relation of MOSFET MF in saturation region can be expressed as:

$$I_{out} = \frac{\beta}{2}\left(V_{cap} - V_{th}\right)^2 \Rightarrow \frac{dI_{out}}{dt} = \sqrt{2\beta I_{out}}\,\frac{dV_{cap}}{dt} \tag{3}$$

in which, $V_{cap} = V_{gs}$ is the voltage of capacitor C, $\beta = \mu C_{ox}\frac{W}{L}$ is the transconductance parameter and V_{th} is the threshold voltage of MOS transistor.

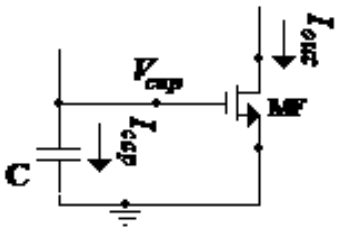


Figure 1: SRD filter principle

Using (3) in (2) and also using equation $I_{cap} = C\frac{dV_{cap}}{dt}$ result:

$$I_{cap} = \sqrt{\frac{I_{tune2}}{I_{out}}} I_{in} - \sqrt{\frac{I_{tune1}}{I_{out}}} I_{out} \tag{4}$$

in which, tuning currents I_{tune1} and I_{tune2} are given by:

$$I_{tune1} = \frac{(C\omega_c)^2}{2\beta} \quad , \quad I_{tune2} = \frac{(AC\omega_c)^2}{2\beta} \ . \tag{5}$$

Eqn. (4) describes the internal nonlinear dynamic operation of the filter; nevertheless, the $I_{out} - I_{in}$ relationship remains linear as described by (2).
The cutoff frequency and dc gain can be written as:

$$\omega_c = \frac{\sqrt{2\beta I_{tune1}}}{C} \quad , \quad A = \sqrt{\frac{I_{tune2}}{I_{tune1}}} \ . \tag{6}$$

The divider-square root- multiplier operator(DSM) is defined as:

$$I_z = \sqrt{\frac{I_{tune}}{I_y}} I_x \ . \tag{7}$$

Therefore the right hand side of eqn. (4) is subtraction of two DSM operators with different inputs and outputs.
Figure. 2 shows the symbol of the DSM operator and Figure. 3 shows the block diagram of the current-mode first-order LPF which consists of two DSM, one capacitor, two MOS transistors (MF1, MF2) and two current mirrors (CM1,CM2).

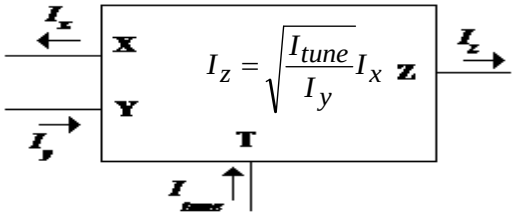


Figure 2: DSM operator symbol

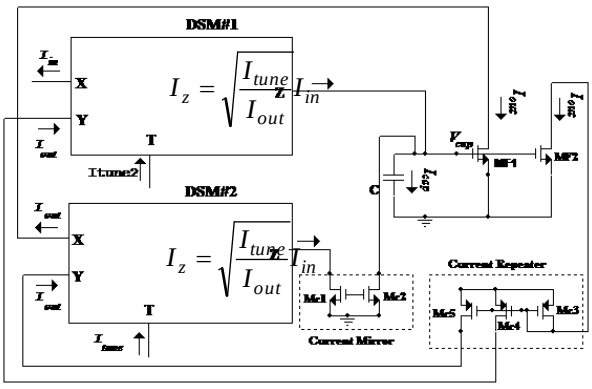


Figure 3: Block diagram of the LPF filter

3. Circuit Design

3.1 Geometric mean

Figure. 4 shows the proposed geometric-mean circuit that consists of two input current mirrors (CM1, CM2), two *Vth*level shifters, two isolating MOS transistors (M7, M8), and a output current mirror (CM3). I_x and I_y are input and I_z is the output of the geometric-mean.

In this circuit, transistors M1, M2, M3 and M4 are identical $\beta_1 = \beta_2 = \beta_3 = \beta_4 = \beta$) and also $\beta_5 = \beta_6$. As the figure shows transistors M1 and M2 of the input current mirrors are always in saturation region and the I-V relationship of them are represented respectively by:

$$V_{g1} - V_{th} = \sqrt{\frac{2I_x}{\beta}} \tag{8}$$

$$V_{g2} - V_{th} = \sqrt{\frac{2I_y}{\beta}} \ . \tag{9}$$

The drain voltages V_{d3} and V_{d4} are determined by:

$$V_{d3} = V_{g2} - V_{th} \tag{10}$$

$$V_{d4} = V_{g1} - V_{th} \ . \tag{11}$$

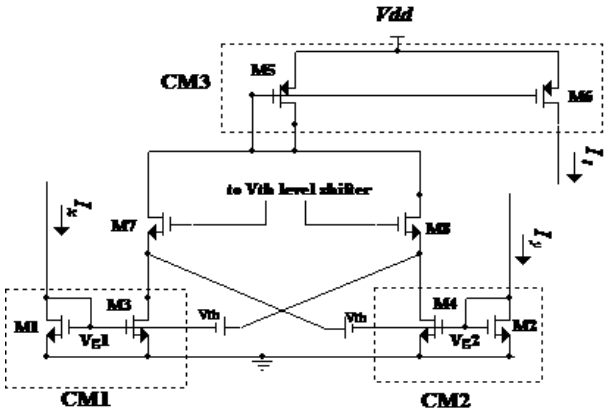


Figure 4: Geometric-mean

The operation regions of transistors M3 and M4 are explained as follows. It can be shown that when input current I_x is higher than input current $I_y (I_x > I_y)$ or equivalently $(V_{g1} > V_{g2})$, transistor M3 operates in triode region andtransistor M4 operates in saturation region. Similarly when input current I_X is less than input current $I_y (I_x < I_y)$ or equivalently $(V_{g1} < V_{g2})$, M4 operates in triode region and transistor M3 operates in saturation region.So the two following cases exist:

Case1:

For $I_x > I_y$, transistor M3 operates in triode region and transistor M4 operates in saturation region so we can write:

$$I_{d3} = \frac{\beta}{2}[\,2(V_{g1} - V_{th})V_{d3} - V_{d3}^2\,] \qquad (12)$$

$$I_{d4} = \frac{\beta}{2}(V_{g2} - V_{th})^2 . \qquad (13)$$

Substituting (10) into (12) results:

$$I_{d3} = \frac{\beta}{2}[\,2(V_{g1} - V_{th})(V_{g2} - V_{th}) - (V_{g2} - V_{th})^2\,] . \qquad (14)$$

The drain current of transistors M5 and M6 can be written as:

$$I_z = I_{d3} + I_{d4} . \qquad (15)$$

Substituting (13) and (14) into (15) gives:

$$I_z = \beta(V_{g1} - V_{th})(V_{g2} - V_{th}) \qquad (16)$$

and substituting (8) and (9) into (16) results:

$$I_z = 2\sqrt{I_x I_y} . \qquad (17)$$

Case 2:

For $I_x < I_y$, transistor M3 operates in saturation region and transistor M4 operates in triode region so we have:

$$I_{d3} = \frac{\beta}{2}(V_{g1} - V_{th})^2 \qquad (18)$$

$$I_{d4} = \frac{\beta}{2}[\,2(V_{g2} - V_{th})V_{d4} - V_{d4}^2\,] . \qquad (19)$$

Substituting eqn. (11) into (19) results:

$$I_{d4} = \frac{\beta}{2}[\,2(V_{g2} - V_{th})(V_{g1} - V_{th}) - (V_{g1} - V_{th})^2\,] . \qquad (20)$$

The drain current of transistors M5 and M6 are expressed as:

$$I_z = I_{d3} + I_{d4} . \qquad (21)$$

Substituting (18) and (20) into (21) gives:

$$I_z = \beta(V_{g1} - V_{th})(V_{g2} - V_{th}) \qquad (22)$$

and substituting (8) and (9) into (22) results:

$$I_z = 2\sqrt{I_x I_y} \qquad (23)$$

As (17) and (23) show in both cases the circuit acts as a geometric-mean.

The squarer/divider is obtained after few modifications by taking the I_y as the output, I_z and I_x as the inputs, and removing the connection between gate and drain of transistor M2 and instead biasing transistor M2 and M4 by connecting their gates to the drain of transistor M8. It results:

$$I_y = \frac{I_x^2}{4I_y} \tag{24}$$

3.2 Vth level shifter

As shown in Figure. 5, the Vth level shifter is realized using MOS transistors ML1, ML2, ML3 and four equal current mirrors I_{b1}, I_{b2}, I_{b3} and I_{b4} $(I_{b1} = I_{b2} = I_{b3} = I_{b4} = I_b)$.

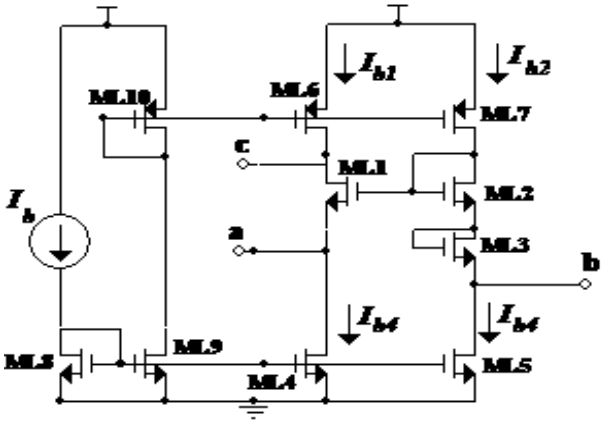


Figure 5: Vth level shifter

The voltage V_{ab} in the figure can be written as:

$$V_{ab} = (-V_{th} - \sqrt{\frac{I_{b1}}{K1}}) + (V_{th} + \sqrt{\frac{I_{b2}}{K2}}) + (V_{th} + \sqrt{\frac{I_{b3}}{K3}}). \tag{25}$$

Assuming that $K_2 = K_3 = 4K_1$, eqn. (25) can be rewritten as:

$$V_{ab} = V_{th} \tag{26}$$

This circuit is used as the V_{th} level shifter of Figure 4.

3.3 Divider-Square root Multiplier

The operation of the Divider-Square root-Multiplier (DSM) as defined in eqn. (7) can be rewritten as:

$$I_z = \sqrt{\frac{I_{tune}}{I_y}} * I_x \Rightarrow I_z = 2\sqrt{\frac{I_x^2}{(4I_y)} * I_{tune}} \ . \tag{27}$$

Eqn. (27) shows that the DSM can be implemented by cascading of, the previously designed squarer/ divider circuit with input currents I_x, I_y and output current $\frac{I_x^2}{4I_y}$, and the geometric-mean circuit with input currents I_{tune},

$\frac{I_x^2}{4I_y}$ and output current I_z.

Figure. 6 shows the block diagram of the DSM. The advantage of cascading a squarer/divider and a geometric-mean with inverse functions is its ability to compensate the non-linearity.

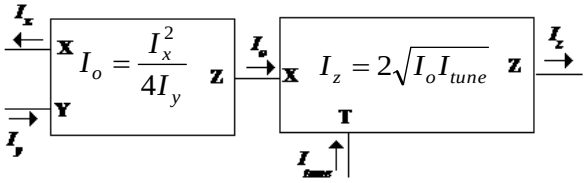


Figure 6: DSM building

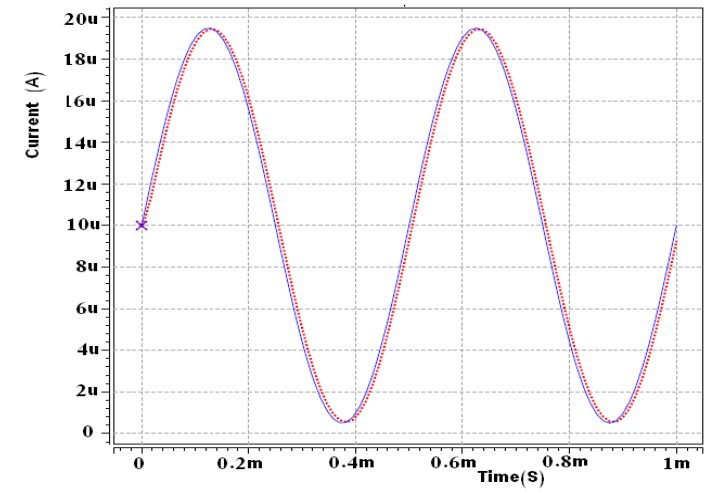
4. Simulation Results

Simulation of the current-mode first order low pass filter of Figure 3 is performed by using HSPICE and with 0.6um AMS CMOS process parameters. $V_{dd} = 2.2V$ and an external capacitor C=1nF were employed. The aspect ratios of the NMOS and PMOS transistors (except for the Vth level shifter transistors ML1, ML2, ML3) were chosen 61.2um/4.8um and 122.4um/4.8um, respectively. The aspect ratio of transistor ML1 in Vth level shifter was chosen 12um/2.4um and for ML2 and ML3 it was 24um/4.8u. As mentioned in section 2, the frequency response of the proposed filter is tunable. Using 15uA for the tune currents I_{tune1} and I_{tune2}, a transient simulation was carried out. Figure 7 shows the time response of the filter for a sinusoidal input current with 19uA peak-to-peak amplitude, DC bias current 10uA and frequency of 2 kHz.

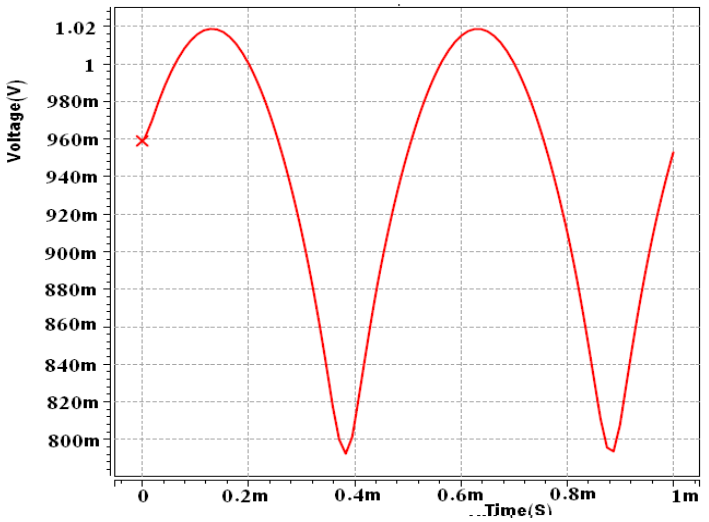
As the figure shows the distortion of the output current is negligible and the input-output current relationship is linear. This is in spite of the fact that the capacitance voltage in the lower half of the signal is strongly distorted, meaning that the system is internally nonlinear. Figure 8 shows the simulation results of the frequency response for different tuning currents, ranging from $I_{tune1} = I_{tune2} =$ 0.4uA to 40uA (from left to right). The results are approximately equal to the expected results from eqn. (6). Figure 9 shows the nonlinear behaviour of the output current by using Total Harmonic Distortion (THD) with a 4096 point Fast Fourier Transform (FFT). The worst-case THD of the output current is less than -51db (0.28%) for the input amplitudes close to the DC current bias. The comparison of the results with those reported in other works [4]-[8], shows 10db lower THD and more tuning current.

5. CONCLUSIONS

Using MOS transistors operating in both saturation and triode regions a new current-mode geometric-mean structure for low voltage square-root domain filters is presented. The proposed circuit has low nonlinearity and high dynamic range. Simulation results of a first-order LPF show that the proposed technique is applicable to design filters with very low voltage requirement. Since the time-dependent state-space equation of a higher-order linear filter can be reduced to a set of first-order differential equations, the technique can be readily extended to the higher order configurations.



(a)



(b)

Figure 7: Time response of the LPF; a: Input and output currents, b: Capacitance voltage

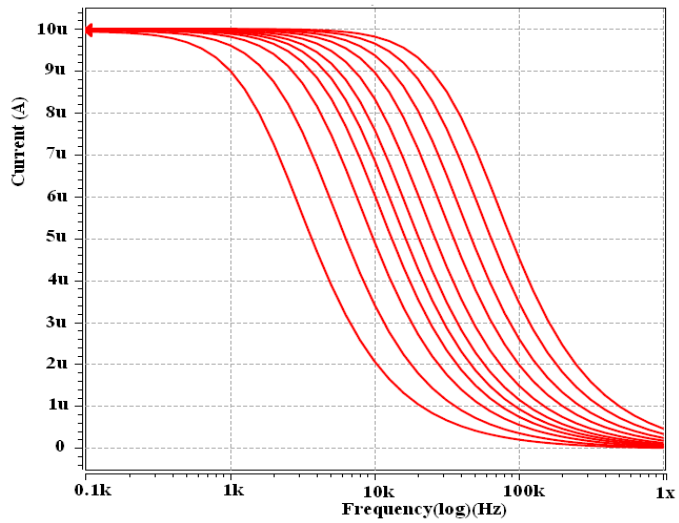


Figure 8: Frequency response of the LPF (for *Itune1* from 0.4uA to 40uA from left to right)

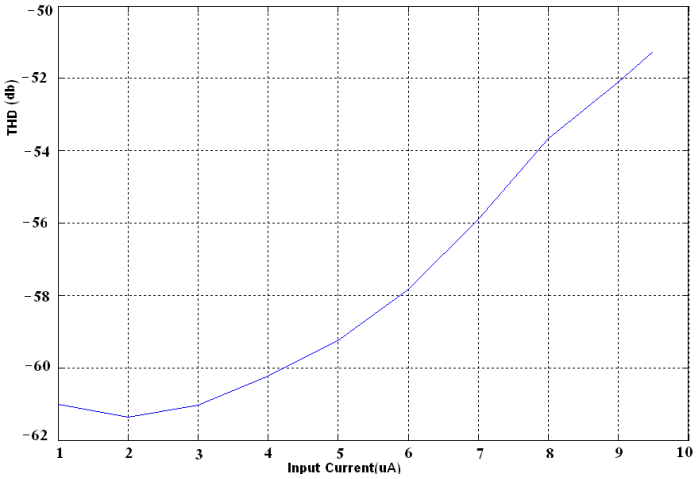


Figure 9: nonlinear performance of the LPF

6. REFERENCES

[1] D. R. Frey, (1996) "Exponential state space filters: A generic current mode design strategy," *IEEE Trans. Circuits Syst. I*, Vol. 43, pp. 34-42.

[2] E. M. Drakakis, A. J. Payne, and C. Toumazou, (1999) "Log-domain state-space: A systematic transistor-level approach for log-domain filtering," *IEEE. Trans. Circuits Syst. II*, Vol. 46, pp. 290-305.

[3] E. Morsy and J. Wu, (2000) "Low voltage micropower log-domain filters," *Analog Integr. Circuits Signal Processing* , Vol. 22, pp. 103-114.

[4] C. A. D. L. C. Blas, A. J. Lopez-Martin and A. Carlosena, (2004) "1.5v tunable square-

root domain filter," *Electron. Lett.* , Vol. 40, No. 4, pp. 133-147.
[5] A. J. Lopez-Martin and A. Carlosena, (2002) "A 1.5v CMOS companding filter," *Electron. Lett.* , Vol. 38, No. 22, pp. 1299-1300.
[6] J. Mulder, A. C. V. D. Woerd, W. A. Serdijn and A. H. M. V. Roermund, (1996) "Current-mode companding √x-domain integrator," *Electron. Lett.* , Vol. 32, No.3, pp.198-199.
[7] R. G. Carvajal, J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, A. G. Galan, A. Carlosena and F. M. Chavero, (2005) "The flipped voltage follower: A useful cell for low-voltage low power circuit design," *IEEE Trans. Circuits Syst. I: Regular Paper,* Vol. 52, No. 7, pp. 1276-1291, 34-42.
[8] C. A. D. L. C. Blas, A. J. Lopez-Martin and A. Carlosena, (2003) "1.5v MOS translinear loops with improved dynamic range and their application to current-mode signal processing," *IEEE. Trans. Circuits Syst. II, Analog Digit. Signal process*, Vol. 50, No. 12, pp. 918-927.
[9] C. Psychalinos and S. Vlassis, (2002) "A systematic design procedure for square-root -domain circuits based on the signal flow graph approach," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl*., Vol. 49, No. 12, pp. 1702-1712.
[10] M. Eskiyerli and Payne, (2000) "Square root domain filter design and performance," *Analog Integr. Circuits Signal Processing,* Vol. 22, pp. 231-243.
[11] E. Seevinck, (1990) "companding current-mode integrator: a new circuit principle for continuous-time monolithic filters, *Electron. Letter*" Vol. 26, pp. 2046-2047.
[12] C. A. D. L. C. Blas, A. J. Lopez-Martin and A. Carlosena, (2004) "Low voltage CMOS nonlinear transconductors and their application to companding current-mode filters," *Analog Integr. Circuits Signal Processing,* Vol. 38, pp. 137-147.
[13] J. Mulder, W. A. Serdijn, A. C. V. D. Woerd, and A. H. M. Roermund, (2000) "Dynamic translinear circuits - an overview, (2002)" *Analog Integr. Circuits Signal Processing,* Vol. 22, pp. 111-126.
[14] C. Psychalinos and S. Vlassis, (2001) "A high performance square-root domain integrator,"*AnalogIntegr. Circuits Signal Processing*, Vol. 28, No. 3, pp. 97-101.
[15] E. Farshidi and S. M. Sayedi, (2007) "A Square-Root Domain Filter Based on a New Geometric-mean Circuit," *15th Iranian Conference on Electrical Engineering ICEE2007*, pp. 6-11.

This paper may be cited as:

Farshidi, E. and Kaiedi, S., 2014. A New Current-Mode Geometric-Mean Structure for SRD Filters. *International Journal of Computer Science and Business Informatics, Vol. 12, No. 1, pp. 100-109.*